The High Short-Term Frequency Stability Digitally Controlled X'tal Oscillator with Small Size and Low Power Consumption

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***Abstract*— NDK have realized the small 9x7 mm size DCXO with a high short-term frequency stability less than 20 ppt for Tau 1 second. By developing a frequency correction control using the digital signal processing with the FPGA and the MCU for our original low-noise small size reference XO. This paper is based on results obtained from "Research and Development Project of the Enhanced Infrastructures for Post 5G Information and Communication Systems" (JPNP20017), commissioned by the New Energy and Industrial Technology Development Organization (NEDO).**

Keywords—DCXO; crystal oscillator; AT-cut; FPGA; MCU;

I. INTRODUCTION

At first, the relationship of the development is shown as follows.

NEDO : The investor of the POST5G project

New Energy and Industrial Technology Development Organization "Research and Development Project of the Enhanced Infrastructures for Post-5G Information and Communication Systems" (JPNP20017)

NICT : The developer of the Wi-Wi system

National Institute of Information and Communications Technology "Wireless Two-Way interferometry" (Wi-Wi) as a new technique to synchronizing clocks.

NDK : The developer of the DCXO

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NICT's co-developer in the Wi-Wi system, providing the key technology, DCXO.

The development process is as follows.

First, NEDO launched an R&D project for an expansion infrastructure for post-5G information and communication systems, for example, smart factories and automated driving.

And next, NICT is the developer of the Wi-Wi system, which will be the basic technology for the post-5G project.

The National Institute of Information and Communications Technology (NICT) aims to construct an extreme time synchronization device and system based on wireless. Two-way interferometry time synchronization technology (Wi-Wi), which requires an oscillator that is compact, low power consumption and has high short-term frequency stability.

And then, NDK is a developer of the DCXO, an essential part of the development of the post 5G project for the Wi-Wi module.

Then, NICT and NDK began the joint development as a project commissioned by NEDO.

The Wi-Wi is a time synchronization technology by using propagation delay time between each module via 920MHz band as shown in the Fig.1.

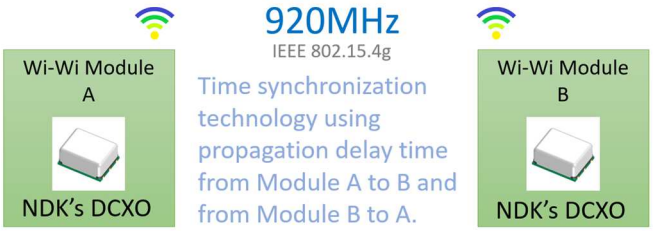


Fig.1. For the precise synchronization by Wi-Wi module [1].

It is important to keep frequency constant on the oscillator for time synchronization.

A high short-term frequency stability allows precise time synchronization because propagation time can be accurately determined.

With this background, NDK began the development of the DCXO.

To achieve the above, NDK used a low-noise reference XO with built-in an AT-cut fundamental crystal resonator and developed the digital signal processing method using a FPGA and a MCU for frequency correction.

The high short-term frequency stability is required from the time synchronization accuracy of the Wi-Wi module.

And the requirements of the Wi-Wi module are as follows.

- Synchronization accuracy: 10 ns
- Synchronization jitter: 10 ps
- Power consumption: 250 mW or less

What important here is to achieve these requirements with as low power consumption as possible.

Since power consumption increases during time synchronization due to RF communication, reducing the frequency of time-synchronization results in lower power consumption.

From this point of view, the target specification of short-term frequency-stability has been set at 20 ppt.

II. METHODS/RESULTS

The concept of the DCXO is consist of three key words.

1. High short-term frequency stability ≦ 20 ppt (τ = 1 sec)
   Stable time synchronization of the Wi-Wi module
   Using the low-noise AT-cut fundamental crystal resonator.
2. Small Size ≦ 300 mm^3
   Be suitable for small modules
3. Low Power Consumption ≦ 40 mW
   Reducing power consumption of Wi-Wi module.

First, the high short-term frequency stability less than or equal to 20 ppt is required as mentioned above.

NDK is working to realize this with the AT-Cut crystal resonator which is suitable for the mass production with low cost because it is needed in the era of POST 5G, huge number of devices will be connecting each other.

Second, small size less than 300 mm^3. This contributes to the miniaturization of the Wi-Wi module.

And the Third, low power consumption less than 40 mW.

These all three elements of the specifications are necessary. The design specifications are shown Table.1.

Table.1. The design specifications of the DCXO.

Specifications	
Short-Term-Stability (τ =1 [sec])	≦ 2×10^{-11}
Size [mm^3] ([mm])	≦ 300 (L 9.5 × W 7.3 × H 4.1)
Power Consumption [mW]	≦ 40
Output Frequency [MHz]	40
Supply Voltage [V]	+3.3 (±5%)
Operating Temperature Range [°C]	-40 to +85
Frequency vs. Temperature Characteristics [ppb]	≦ ±20
Output Waveform	LVCMOS
Output Load Capacitance	15 [pF]

The previous system design is shown Fig.2., before presenting current system design.

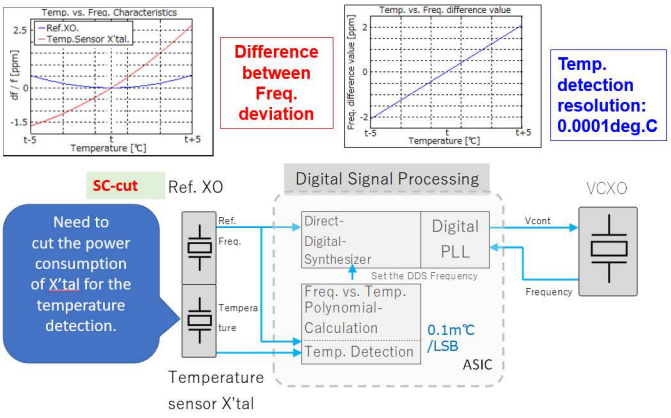


Fig. 2. The previous system design [2][3].

In the previous system, three crystal oscillators were used in it, the one of which was used to detect temperature of the reference XO.

The system can detect temperature precisely and can correct frequency vs. temperature characteristics in the Ref. XO, but the temperature sensor X'tal consumes some power. (It was 15 mW.)

That was a problem.

Power consumption must be lower and short-term frequency stability must also be improved.

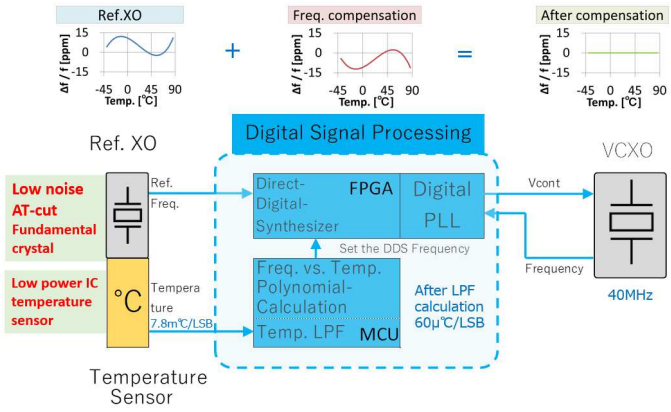


Fig. 3. The current system design.

To ensure the concept, it is indicated as a block-diagram of Fig.3. above.

A temperature sensor is an IC sensor used in place of X'tal temperature sensor for reducing the power.

This system will be able to achieve the high frequency accuracy without any heater like as an OCXO.

The system is made of three parts of function blocks.

Explaining from input block at first, the reference low noise X'tal oscillator that of made by an AT-cut fundamental crystal resonator.

And that frequency is input to the digital signal processing block consist of the FPGA and the MCU.

And the temperature sensor near by the reference XO detects the reference XO's body temperature as a crystal resonator's temperature.

The output value from the temperature sensor is input to the low-pass filter. Then, the polynomial calculation of the frequency vs. temperature characteristic of the reference XO is applied.

Then, the calculated polynomial compensation values by the temperature are input to the DDS.

Then, PLL operation is performed using the reference frequency created by DDS.

Thus, the VCXO frequency is constant nonetheless of the temperature be fluctuated within the range of -40 to +85 deg.C.

The development process is as follows.

1. High short-term frequency stability ≦ 20 ppt (τ = 1 sec)

To improve Allan-Deviation, the following design process (1) and (2) were done and followed by (3).

(1) To design the DDS resolution to 20 ppt / LSB, then match temperature detection resolution to the DDS resolution.

Short-term frequency stability is expressed as Allan-Deviation of Equation.1.

$$\text{Allan-deviation} = \sqrt{\text{Allan-variance}}$$

$$\text{Allan-variance} = \sigma_y{}^2(\tau, m) = \frac{1}{m}\sum_{j=1}^{m}\frac{1}{2}(y_{k+1} - y_k)^2{}_j$$

Equation.1. Allan-Deviation [4][5].

The smaller ($y_{k+1} - y_k$) values are better. And it is determined from the resolution of the DDS and fluctuating period.

So, we designed the DDS as follows.

(1)-1 DDS control resolution

20 [ppt / LSB]

The 20 ppt is corresponding to the value of ($y_{k+1} - y_k$).

(1)-2 Resolution of the temperature compensation

20 [ppt / 60 μ℃] (= 1 ppb / 3 m℃)

It is determined from the frequency vs. temperature characteristics of the Ref. XO at 25 deg.C. (See. Fig.4.)

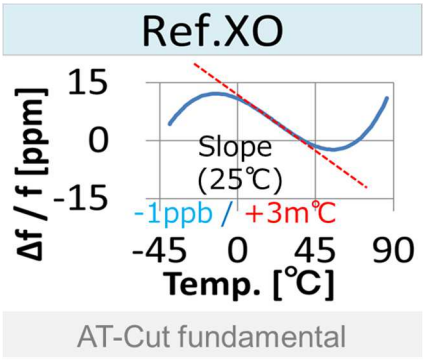


Fig. 4. The frequency vs. temperature characteristics of the Ref. XO at 25 deg. C.

(1)-3 To convert temperature sensor detection values to high resolution by LPF calculation.

Temp. Sensor Resolution	: 7.8 [m℃ / LSB]
After LPF calculation	: 60 [μ ℃ / LSB]

(1)-4 To fit the temperature compensating resolution of the After LPF calculation of the temperature sensor value to the DDS control resolution of 20 [ppt / LSB].

(2) To measure Allan-Deviation with LDO for the power supply of the Ref. XO

The frequency stability of the Ref. XO depends on the noise applied via its power supply. Therefore, it must confirm that the Allan-Deviation value of the Ref. XO is sufficiently low at tau is one second even when the Ref. XO is powered from a small LDO that can be mounted on a DCXO board.

The measurement result of the Allan-Deviation value of the Ref. XO was 12 ppt when it powered from the LDO and from 6 to 8 ppt when it powered from external power unit as shown in Talble.2. That difference between these values indicates the difference in power supply noise.

Table.2. The difference in Allan-Deviation due to difference in power supply noise.

Measured value	Power Supply (LDO or Power Unit)	
	LDO 120nV/√Hz (@10Hz)	Power Unit 50n V /√Hz (@10Hz)
Allan-Deviation at Ref.XO. output (τ=1sec)	12 ppt	6～8 ppt -87 ～ -80 dBc / Hz (offset 1Hz)

(3) To reduce the power fluctuation caused by the logic device.

In the actual DCXO, it is necessary to consider the effect of temperature fluctuations caused by logic devices, especially the FPGA, on the Ref. XO frequency.

Fig.5. shows the effect of heat fluctuation in the logic device on the Ref. XO. Even if the range of fluctuation is 3 milli-deg.C the frequency fluctuation on the Ref. XO corresponds to the 1 to 1.5 ppb. (See also Fig. 4.)

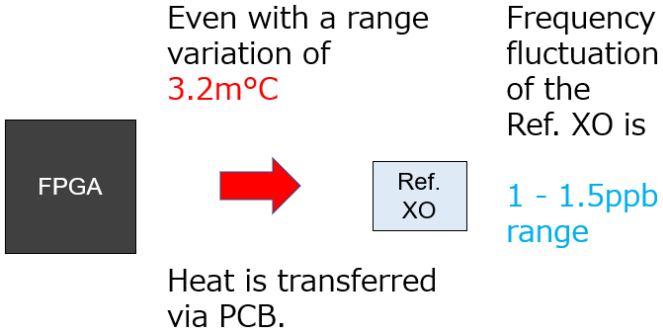


Fig.5. The effect of heat fluctuation in the logic device on the Ref. XO

Fig. 6 shows the locations of temperature fluctuations and the cause in the logic device. In the DCXO developed this time, the Phase Detector block was the point of power fluctuation, which had triggered by the interpolation operation of the frequency control input value for the DDS in the previous stage.

The clock for the interpolation operation for the DDS input value is CLK_DDS shown in Fig.6.

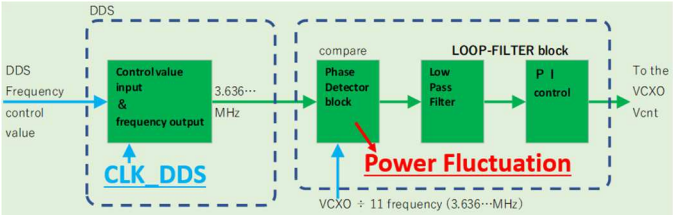


Fig.6. The location of power-consumption-fluctuation and the cause in the logic device.

To increase the control resolution of DDS, the interpolated clock should be faster. However, it causes power fluctuations to increase.

The power fluctuation in the Phase Detector block caused by the interpolation for the input value of the DDS have caused the temperature fluctuation of the Ref. XO, which was the cause of the frequency fluctuation of the Ref. XO.

Fig.7. shows the test values input to the DDS to confirm this, and Fig.8. shows the measurement results. Test values were input to the DDS repeatedly.

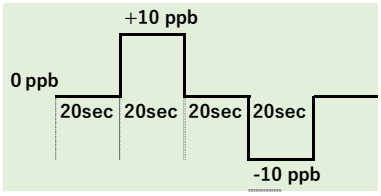


Fig.7. Test input values to the DDS.

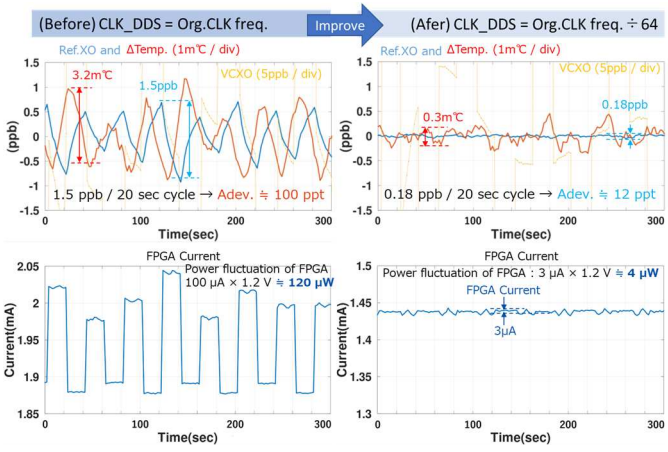


Fig.8. The measurement result of power fluctuation.

The left side in the Fig.8. shows the result before improvement and right side shows the one after improvement. The improvement was to slow down the clock of DDS from the original CLK frequency to one sixty-fourth.

And the upper row is the plot of the Ref. XO frequency and temperature fluctuation of the Ref. XO and VCXO frequency.

The Ref. XO is blue plot, temperature fluctuation is red plot, and the VCXO is orange plot.

With the plot, the current consumption of the FPGA is shown in the lower graph. These all values are measured simultaneously.

From the measurement result, it has reduced in the fluctuation of the Ref. XO frequency and the temperature fluctuation, obviously.

Thus, by slowing down the interpolation clock for the input value of the DDS, the frequency fluctuation of the Ref. XO was reduced.

Fig.9. shows the Allan-Deviation transition of the VCXO output frequency as a plot and it was 18 ppt at tau 1 second. (The frequency measurement was done under the still air condition.)

This value is calculated and plotted by continuously measuring the output frequency for 2100 seconds with a 1 second gate time and then shifting the selected range of 100 consecutive point intervals in the measurement by 1 point toward end point of the data.

(ex. as for 1st period, applied Data Points 1 – 100 seconds, as for 2000th, applied Data Points 2001 – 2100 seconds)

The reason for this is to check the instantaneous value fluctuations of the Allan-Deviation.

The instantaneous values fluctuation did not occur, and the results was good.

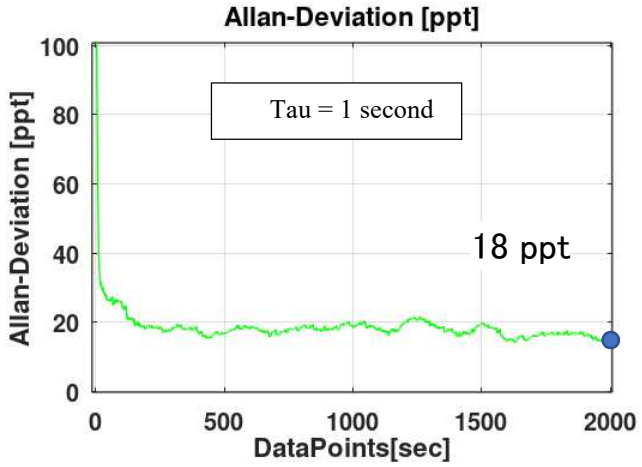
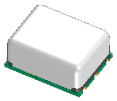


Fig. 9. Allan Deviation of the DCXO.

2. Small Size ≦ 300 mm^3

The shape of the DCXO is shown in Fig.10. The size is 284 mm^3, designed smaller than 300 mm^3.



284 mm^3
L 9.5 × W 7.3 × H 4.1

Fig.10.The Size of the DCXO.

3. Low Power Consumption ≦ 40 mW

Power consumption is currently 51 mW and does not reach 40 mW. The following changes are being considered to achieve the design specification.

- The discrete Buffer IC will be removed and configured into an ASIC to further reduce power consumption by lowering the voltage.
- Furthermore, power consumption will be reduced by integrating the MCU and the FPGA into one-chip device.

The temperature characteristics are within ±20 ppb in the range of -40 deg.C to +85 deg.C for 5 samples as shown in Fig.11.

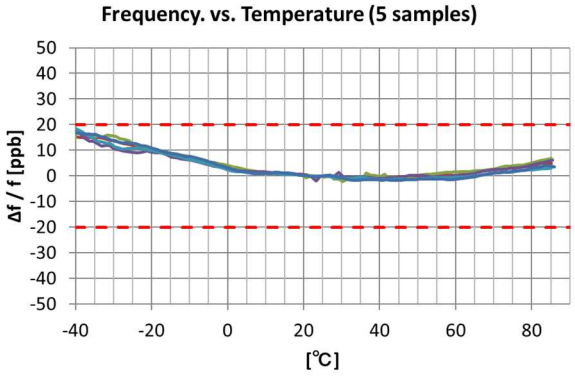


Fig. 11. The frequency vs. Temperature characteristics of the DCXO.

The results are summarized in Table 3.

Table.3. A Summary of the results.

Specifications		
Short-Term-Stability (τ =1 [sec])	≦ 2×10^{-11}	☑ Achieved
Size [mm^3] ([mm])	≦ 300 (L 9.5 × W 7.3 × H 4.1)	☑ Achieved
Power Consumption [mW]	≦ 40	☐ Improving
Output Frequency [MHz]	40	-
Supply Voltage [V]	+3.3 (±5%)	-
Operating Temperature Range [°C]	-40 to +85	-
Frequency vs. Temperature Characteristics [ppb]	≦ ±20	☑ Achieved
Output Waveform	LVCMOS	-
Output Load Capacitance	15 [pF]	-

III. DISCUSSION/INTERPRETATION

A Summary of the power fluctuation caused by logic device is shown in Table.4.

Table.4. A summary of the CLK_DDS vs. freq. fluctuation on the Ref. XO.

CLK_ DDS (interpo lation) [Hz]	Power Dissipation of the FPGA [μW]	Temperature fluctuation range of the Ref. XO. [m℃]	Frequency fluctuation range of the Ref. XO. [ppb]	Allan-deviation at Ref. XO. [ppt]	Note
Original CLK freq.	120	3.2	1.5	100 (NG)	> 20 ppt of Allan-deviation by FPGA power fluctuation.
Original CLK freq. ÷ 64	4	0.3	0.18	12 (OK)	The impact of powe fluctuations on FPGAs has decreased.

The temperature fluctuation range of the Ref. XO and frequency fluctuation range of the Ref. XO was equal to the one slope of the frequency vs. temperature characteristics of the Ref. XO at 25 deg.C. (See Fig. 4.)

That indicates that main cause of the frequency fluctuation of the Ref. XO is caused by the temperature fluctuation, and it comes from the temperature fluctuation of the FPGA, and it is effective to reduce the power fluctuation of the logic device in the FPGA.

This improvement has resulted in better short-term frequency stability expressed as Allan-Deviation.

IV. CONCLUSIONS

The followings are the conclusions.

1. High short-term frequency stability of 20 ppt at tau 1 second, which is required for Wi-Wi modules, has been achieved with this design, especially the reduction of frequency fluctuation of the Ref. XO due to the reduction of power fluctuation of the logic device.
2. Small Size 300 mm^3 has been achieved.
3. Power Consumption is necessary to improve. NDK suppose that 40 mW, the target of power consumption, would be achieved by single-chip ASIC of combined FPGA and MCU.
4. Frequency vs. Temperature characteristics within the range of ±20 ppb has been achieved.

As a DCXO for post-5G extremely precise time synchronization by Wi-Wi, NDK have achieved high short-term frequency stability DCXO. NDK is aiming to achieve the specification of the power consumption. This is because Wi-Wi, of course, can also contribute to reducing environmental load.

REFERENCES

[1] Horizontal Atmospheric Delay Measurement Using Wireless Two-Way Interferometry (Wi-Wi) - Yasuda - 2019 - Radio Science - Wiley Online Library https://agupubs.onlinelibrary.wiley.com/doi/full/10.1029/2018RS006770

[2] Yasuto Ishii, Kaoru Kobayashi, Tsukasa Kobata, Manabu Ito, Shigenori Watanabe, Shinichi Sato, Kazuo Akaike, “A NEW GENERATION DSP-OCXO USING CRYSTAL TEMPERATURE SENSOR”, International Frequency Control Symposium, IEEE,, 2012.

[3] Kaoru Kobayashi, Yoshiaki Mori, Tsukasa Kobata, Manabu Ito, Shigenori Watanabe, Shinichi Sato, Kazuo Akaike, "High-performance DSP-TCXO using twin-crystal oscillator", International Frequency Control Symposium, IEEE,, 2014.

[4] Allan Variance -- Overview by David W. Allan (allanstime.com) http://www.allanstime.com/AllanVariance/

[5] John R. Vig. “Quartz Crystal Resonators and Oscillators -For Frequency Control and Timing Applications – A Tutorial January 200